CECS eNEWS

Volume 2, Issue 3, July 2002

Center for Embedded Computer Systems, University of California, Irvine

Highlights

Inside this issue:

CECS at CODES '02

The Center for Embedded Computer Systems (CECS) at the University of California, Irvine continues playing a dominant role at the 10th International Symposium on Hardware/ Software Co-Design (CODES '02) held at Estes Park, CO on May 6-8, 2002. This is following its dominant role at the Design, Automation and Test in Europe Conference (DATE 02) held March 4—8, 2002 in Paris, France. (see CECS eNEWS Volume 2, Issue 2, April 2002)

The following technical presentations were made by CECS faculty affiliates and their graduate students at CODES '02 and the technical papers can be found in the conference proceedings at the cited pages:

- "Codesign-Extended Applications", Brian Grattan, Greg Stitt, and Frank Vahid, pp 1—6
- "Multi-Objective Design Space Exploration Using Genetic Algorithms", Maurizio Palesi and Tony Givargis, pp 67—72
- "Communication Speed Selection for Embedded Systems with Networked Voltage-Scalable Processors", Jinfeng Liu, Pai H. Chou, and Nader Bagherzadeh, pp 169—174
- "Energy Frugal Tags in Reprogrammable I-Caches for Application-Specific Embedded Processors", Peter Petrov and Alex Orailoglu, pp 181—186

There were 36 published papers in the proceedings and CECS research affiliates had 4 for an 11% contribution rate.

Professor Daniel D. Gajski delivered an invited luncheon talk titled "System-Level Semantics:

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CECS at DAC

The Center for Embedded Computer Systems (CECS) at the University of California, Irvine had the following presence at the 39th Design Automation Conference (DAC) in New Orleans, LA from June 10—14, 2002. This year's DAC technical program had an emphasis on embedded systems plus the second annual Embedded Systems Showcase offered exhibitors and attendees a highly focused area to display and view the latest tools for the design of embedded systems-on-chip (SoC). DAC's continuing emphasis on embedded systems reassures CECS that our embedded systems research programs are timely, relevant, and important to our nation's technical posture and economic wellbeing.

The following technical papers

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SoC design by CECS

Seminar Announcement

The Center for Embedded Computer Systems (CECS) is pleased to announce the *2002 Southern California Embedded Systems Seminar* to be held on September 10, 2002 at the Jazz Semiconductor Auditorium, Newport Beach, CA.

The technical program is currently under organization but will consist of 8 CECS research affiliates making technical presentations, an industrial panel will discuss future engineering challenges in embedded systems, and the Luncheon Speaker will be Dr. Justin Harlow, Semiconductor Research Corporation.

Please watch our web site, *www.cecs.uci.edu*, for detail program information and free registration procedures. This should be an exciting day devoted to leading edge design and technology issues associated with embedded systems. We look forward to your attendance and participation in reviewing our research activities and discussing your technical problems and concerns.

Colloquium

The following colloquia are being held in the CECS Conference Room 127:

- 2:00 pm, July 24, 2002, "Polychrony for System Design", Jean-Pierre Talpin, INRIA Project ESPRESSO, France

- 3:00 pm, July 25 and 26, 2002, "Tutorial on Real Time Operating Systems: Basics and Actual Trends", Dr. Franz J. Rammig, University of Paderborn, Germany

Book Review

Specification and Design Methodology for Real-Time Embedded Systems

Randall S. Janka

Kluwer Academic Publishers
2002

Dr. Randall S. Janka received his PhD from the Georgia Institute of Technology in 1999. This book is an update and expansion on his doctoral dissertation. The foreward to this book is written by Professor Daniel D. Gajski who was inspirational in motivating Dr. Janka's research.

This technical book outlines and compares the various Specification and Design Methodologies (SDM). He then develops a design methodology termed Methodology Applying Generation, Integration, and Continuity (MAGIC) which is an extension of Gajski's Specify-Explore-Refine (SER) methodology. He concludes by discussing a case study applying the MAGIC methodology to the DARPA Rapid prototyping of Application Specific Signal Processors—Synthetic Aperture Radar (RASSP SAR) example.

This well written technical book is a comprehensive presentation of the present development status of the Specify and Design Methodology (SDM).

Best Paper Award

At the recent 39th Design Automation Conference in New Orleans, LA, Professors Fadi J. Kurdahi and Nader Bagherzadeh received the 2002 IEEE Circuits and Systems VLSI Transactions Best Paper Award from Professor Josef A. Nossek, President of the IEEE Circuits and Systems Society. This award was granted for the paper "A Framework for Reconfigurable Computing: Task Scheduling and Context Management", R. Maestre, F. J. Kurdahi, M. Frenandez, R. Hermida, H. Singh, and N. Bagherzadeh, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 9, No. 6, December 2001, pp 858-873. The recipients received an IEEE Certificate and a cash prize. Congratulations Professor Kurdahi and Professor Bagherzadeh on this IEEE recognition of your research activities!

This best paper award marks the second time in less than five years that faculty affiliated with the Center for Embedded Computer Systems have won the award. Professors Daniel Gajski and Frank Vahid won this Best Paper Award in 1998 for the paper "SpecSyn: An Environment Supporting the Specify-Explore-Refine Paradigm for Hardware/Software System Design", Frank Vahid, Sanjiv Narayan, Jie Gong, and Daniel Gajski, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 6, No. 1, March 1998, pp 84-100.

"It is most rewarding to see the Center for Embedded Computer Systems receive international recognition for the outstanding research results accomplished by the faculty, students, and research associates," says Dean Nicolaos G. Alexopoulos of the Henry Samueli School of Engineering. "These two best paper awards are tangible evidence of the Center's excellence." These Best Paper Awards are symbolic recognition of the excellence and quality in research performed at the Center for Embedded Computer Systems. Our historic and continuing commitment to leading edge research in embedded systems is a passion that we continually strive to instill in all our graduate students.

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Contracts

- Professor Daniel D. Gajski received a gift to support his system level design for communications research program from Conexant Systems, Inc. Newport Beach, CA

- Professor Rajesh K. Gupta received a $40,000 travel grant from National Science Foundation for U.S. - France Cooperative Research project

Professor Profile

CECS is proud to profile Associate Professor Alexander V. Veidenbaum, Department of Information and Computer Science , University of California, Irvine (UCI), as an outstanding research affiliate. He serves as Director of the Hardware and Systems Laboratory at CECS. Professor Veidenbaum was born in St. Petersburg, Russia and received a PhD from the University of Illinois at Urbana-Champaign in 1985. He was an Assistant Professor in the Department of Computer Science at the University of Illinois at Urbana-Champaign from 1985 to 1994. He was also a member of the technical staff at the Center for Supercomputing where he was one of the principal designers of the Cedar multiprocessor and its successors. From 1994 to 1995 he was the Director of Technology at the International Supercomputing Technology in Mulhose, France where he led the development of another highly parallel computing system funded by the European community. From 1995 to 1998 he was an Associate Professor at the University of Illinois in Chicago and joined the UCI faculty in 1999.

Professor Veidenbaum's research interests are hardware and systems, including building computer systems, computer architecture, and compiler design. He has made significant contributions in the areas of memory hierarchy and cache design, adaptive system architecture, and multiprocessing systems. He recently spent a year in industry developing systems for optimizing the delivery of IP-based data over mobile and cellular networks. (see CECS eNEWS Volume 2, Issue 2, April 2002, page 2)

Professor Veidenbaum's current research focuses on designing systems with low energy consumption, for both high-performance and embedded domains, systems for mobile network infrastructure, and high-performance architecture.

Professor Veidenbaum is the author of more then 40 technical publications in refereed conferences and journals. The following are a sample of his recent publications:

- "Power-Efficient Instruction Fetch Architecture for Superscalar Processors", Ana-Maria Badulescu and Alex Veidenbaum, Proceedings on Parallel and Distributed Processing Techniques and Architectures (DDPTA), June 25-27, 2002

- "Adapting Cache Line Size to Application Behavior", Alexander V. Veidebaum at el, Proceedings of the International Conference on Supercomputing, June 1999, pp 145-154

Prof. Alex Veidenbaum with the Adaptive Memory Hierarchy board he designed for a DARPA funded project.

Visitor Profile

CECS is honored to host for the months of June, July, and August a Visiting Researcher, Professor Franz J. Rammig, Universitaet Paderborn, Germany. He was born in Landsberg/Lech, Bavaria and received his MSc degree in Mathematics from Universitaet Bonn, Germany in 1973, and the Dr. rer. nat. degree in Informatics from Universitaet Dortmund, Germany in 1977.

Since 1983, Professor Rammig has been a professor for Practical Informatics at University of Paderborn and recipient of a donated chair at the Heinz Nixdorf Instit, an interdisciplinary research institute concentrating on Informatics, Mechanical Engineering, Electrical Engineering, and Economics. He is currently serving as the Chairman of the Heinz Nixdorf Instit. Professor Rammig also serves as CoDirector of C-LAB which is a collaborative research and development laboratory between University of Paderborn and Siemens AG. C-LAB has approximately 70 scientists and 120 graduate students performing comprehensive research in Distributed Computing. Professor Rammig is also a member of the Board of Directors of the Paderborn Center for Parallel Computing, one of Germany's most prestigious research institutes in Parallel Computing.

In 1998-1999, he served as Vice President of the German Informatics Society. He has been very active in the International Federation for Information Processing (IFIP) representing Germany and serving on numerous working groups. His efforts were recognized in 1998 when he received the IFIP Silver Core Award. Professor Rammig is a member of the Editorial Board of the Journal of Network and Computer Applications and Teubner Texte zur Informatik, a series of German monographs.

The research interests of Professor Rammig are focused on the design process for distributed embedded real-time systems. This includes abstract specification methodologies, modeling techniques, synthesis and verification, hardware/software codesign, real-time operating systems, and real-time communications systems. He is the author of over 80 technical publications and the following are three of his most recent publications:

- "Customizing the Configuration Process of an Operating System Using Hierarchy and Clustering", Ramakrishna Cirvukula, Carsten Boeke, and Franz J. Rammig, Proceedings of the 5th IEEE International Symposium on Object-Oriented Real-Time Computing (ISORC 2002), April 29—May 1, 2002, pp 280-287

- "OCL Goes Real-Time", Franz J. Rammig, Proceedings of the 5th IEEE International Symposium on Object-Oriented Real-Time Computing (ISORC 2002), April 29—May 1, 2002, pp 423-424

- "Synthesis Aspects of the PARADISE Design Environment", Franz J. Rammig, Proceedings of the 7th IEEE International Workshop on Object-Oriented Real-Time Dependable Systems (WORDS 2002), January 7-9, 2002, pp 27-34

PUBLICATIONS

The following were published by CECS faculty affiliates during the period of April 1, 2002 to June 30, 2002:

Focus	Title, Authors, Publication
CoDesign	"Codesign-Extended Applications", Brian Grattan, Greg Stitt, and Frank Vahid, Proceedings of the 10th International Symposium on Hardware/Software CoDesign, May 6-8, 2002, pp 1—6
Design Space Exploration	"Multi-Objective Design Space Exploration Using Genetic Algorithms", Maurizio Palesi and Tony Givargis, Proceedings of the 10th International Symposium on Hardware/Software CoDesign, May 6-8, 2002, pp 67—72
Communication Speed Selection	"Communication Speed Selection for Embedded Systems with Networked Voltage-Scalable Processors", Jinfeng Liu, Pai H. Chou, and Nader Bagherzadeh, Proceedings of the 10th International Symposium on Hardware/Software CoDesign, May 6-8, 2002, pp 169—174
Reprogrammable Caches	"Energy Frugal Tags in Reprogrammable I-Caches for Application-Specific Embedded Processors", Peter Petrov and Alex Orailoglu, Proceedings of the 10th International Symposium on Hardware/Software CoDesign, May 6-8, 2002, pp 181—186
Memory Profiler	"A Fast On-Chip Profiler Memory", Roman Lysecky, Susan Cotterell and Frank Vahid, Proceedings of the 39th Design Automation Conference, June 10-14, 2002, pp 332—337
High-Level Synthesis	"Coordinated Transformations for High-Level Synthesis of High Performance Microprocessor Blocks", Sumit Gupta, Timothy Kam, Shai Rotem, Nick Savoiu, Nikil Dutt, Rajesh Gupta, and Alex Nicolau, Proceedings of the 39th Design Automation Conference, June 10—14, 2002, pp 875—881
System Level Design	"System Level Design Using SpecC Profiler", Lukai Cai and Daniel Gajski, UCI CECS Technical Report 02-08, April 1, 2002
Matrix Multiplication	"RTL Design and Synthesis of Sequential Matrix Multiplication", Pei Zhang and Daniel Gajski, UCI CECS Technical Report 02-09, April 3, 2002
Scheduling	"Scheduling in RTL Design Methodology", Dongwan Shin and Daniel Gajski, UCI CECS Technical Report 02-11, April 11, 2002
Queue Generation	"Queue Generation Algorithm for Interface Synthesis", Dongwan Shin and Daniel Gajski, UCI CECS Technical Report 02-12, April 11, 2002
Interface Synthesis	"Interface Synthesis from Protocol Specification", Dongwan Shin and Daniel Gajski, UCI CECS Technical Report 02-13, April 11, 2002
Model Refinement	"Automatic Model Refinement for Fast Architecture Exploration", Junyu Peng, Samar Abdi, and Daniel Gajski, UCI CECS Technical Report 02-14, April 1, 2002
System Design	"Interactive System Design Flow", Junyu Peng, Lukai Cai, Andreas Gerstlauer and Daniel Gajski, UCI CECS Technical Report 02-15, April 1, 2002
Modeling Guidelines	"SpecC Modeling Guidelines", Andreas Gerstlauer, UCI CECS Technical Report 02-16, April 16, 2002
Parallelization Optimization	"Parallelization Optimization of System-Level Specification", Lukai Cai and Daniel Gajski, UCI CECS Technical Report 02-18, June 1, 2002
Memory Exploration	"A Framework for Memory Subsystem Exploration", Prabhat Mishra, Mahesh Mamidipaka, and Nikil Dutt, UCI CECS Technical Report 02-19, May 24, 2002
Specification Tuning	"Specification Tuning of System Level Design", Lukai Cai and Daniel Gajski, UCI CECS Technical Report 02-20, June 6, 2002
Task Scheduling	"Energy Aware Task Scheduling with Task Synchronization for Embedded Real Time Systems", Ravindra Jejurikar and Rajesh Gupta, UCI CECS Technical Report 02-21, June 21, 2002

Interview

On July 2, 2002, CECS *eNEWS* had the privilege to interview Dr. Frank Micheletti, Manager, External Technologies Development, Conexant Systems, Inc., Newport Beach, CA. The discussion ranged over a broad spectrum of business and technical issues: student internships, technology transfer cooperation, collaborative research paradigms, intellectual property, and future technology thrusts and challenges. The following is an extraction of relevant comments he made during the CECS interview:

- *eNEWS*: What is your perspective of future embedded systems with regard to communications applications?

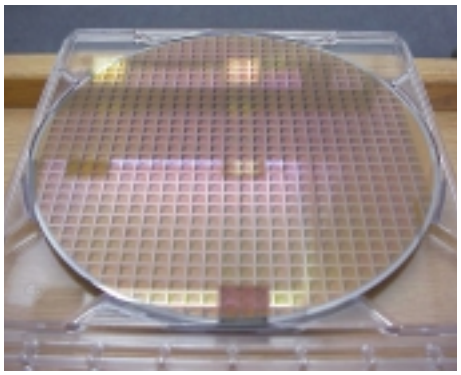
☻ Micheletti: The level of functional integration and feature enhancements in our products will continue to increase which will exacerbate the embedded software content of future embedded systems. This demand for new features and emerging standards continues the trend of stressing the software content of product design. Future hand held products will contain embedded video features which will impact power requirements and packaging.

- *eNEWS*: What are Conexant's anticipated future engineering thrusts?

☻ Micheletti: We plan to continue the development of multichip subsystems to support system-in-package (SiP) technology. It is anticipated that these new concepts will be based on the foundations employed in present Conexant SiP subsystem technology and methodology. Another important future thrust will be in home networking applications supporting smart appliances and interactive entertainment systems. Finally, our recent acquisition of Globespan Virata's video compression business is based on our belief that video will be a large part of the personal communications devices in the next decade, both wireline and wireless.

- *eNEWS*: What is Conexant's desired relationship with CECS?

☻ Micheletti: We, of course, are always looking for outstanding new employees and would like to continue expanding student intern programs and technology exchanges with CECS. Further, we would like to develop more collaborative research programs to validate the emerging system-level design tools developed at CECS on real industrial applications.



- *eNEWS*: What technology role does Conexant expect CECS to play in the future?

☻ Micheletti: We would like to see improvements in predictive hardware/software exploration and optimization techniques to allow better trade-offs in the initial stages of the design process. And, of course, we always hope to see CECS continue to develop innovative design methodologies to increase designer productivity. Although the present relationship is primarily with Conexant Systems, I would like to see the CECS relationship expanded in the future to include Mindspeed Technology and Skyworks Solutions.

Interview conducted by Bob Larsen

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What is needed and what is not needed?"

Professor Rajesh Gupta served as Program Co-Chair and Professors Pai Chou, Daniel Gajski, Rajesh Gupta, Alex Orailoglu, and Frank Vahid served on the Technical Program Committee. This 12% level of participation in conference organization is very high for one research entity.

CECS's influence will continue next year at CODES '03 as Professor Rajesh Gupta will serve as Conference General Co-Chair and Professor Pai Chou will serve as Program Co-Chair.

CECS is extremely proud of its technical influence at CODES '02 and DATE '02 which reflects the level of technical relevance and recognition in its collaborative research programs.

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were made by CECS faculty affiliates and their graduate students with the cited pages from the conference proceedings:

- "A Fast On-Chip Profiler Memory", Roman Lysecky, Susan Cotterell and Frank Vahid, pp 332-337

- "Coordinated Transformations for High-Level Synthesis of High Performance Blocks", Sumit Gupta, Timothy Kam, Michael Kishinevsky, Shai Rotem, Nick Savoiu, Nikil Dutt, Rajesh Gupta and Alex Nicolau, pp 875—881

Professor Nikil Dutt served as Chair of the technical session titled "Memory Management and Address Optimization in Embedded Systems" and Professor Rajesh Gupta served as Chair of the technical session titled "Theoretical Foundations of Embedded System Design". Professor Frank Vahid served as an Organizer and Presenter at a tutorial titled "New Computing Platforms for Embedded Systems".

CECS—Solving Tomorrow's Problems!

Center for Embedded Computer Systems, University of California, Irvine

CECS Mission Statement:

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

CECS Research Advisory Board
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Design Spies

Since September 11, 2001, I have been intrigued with the concept of spying. Could our spying network have prevented this horrendous national tragedy? The signals were there, but nobody in any police agency could suppress all the surrounding noise and detect the terrorist's plans. The intrigue of spying has been the subject of numerous novels and movies.

Spying is defined by Webster's as: *to watch closely and secretly*. Does the concept of spying have any role in the creative SoC design process?

Recently I was reading about Atrenta's SpyGlass 3.0 tool. SpyGlass 3.0 provides customization of the analysis function so the designer can add rules, enable and disable tests, and establish profiles that store selection policies, rules, and parameters. The designer can choose among various policy and rule sets that are organized by functional and performance requirements, by application selection, and vendor-specific rules.

SpyGlass 3.0 also performs testability analysis at the RTL level and includes rules for automatic test-pattern generation and built-in-self test. By writing RTL code that complies with testability rules, the designer can save considerable synthesis and simulation time while producing functional blocks that are easier to reuse.

The concept of design spying sounds intriguing while providing an opportunity for increasing designer productivity, design quality, and time-to-market. By employing rules and policies, design spying can be made adaptable to any application and design level. Design spying can also improve the learning curve for novice designers.

Spy engines could be created to concurrently or periodically check for design violations at the behavioral, structural, and physical levels of design. The use of design spying would catch design violations early; thus making corrective action much less painful and more economical.

I believe rule, profile, and policy based design spying could have profound cost/time impact on the SoC design and test process!

Bob Larsen